What is claimed is:

1. ~~A system comprising:~~

a bus;

a resource coupled to the bus; and

a plurality of entities coupled to the bus, at least one entity among the plurality of entities including a memory, wherein at least a portion of the memory of the at least one entity is selectively reset when the at least one entity has access to the resource.

2. The system of claim 1, wherein the at least one entity is an integrated circuit.

3. The system of claim 1, wherein the resource includes at least a portion of a memory device.

4. The system of claim 1, further comprising a manager to manage at least one request from the plurality of entities to access the resource.

5. The system of claim 1, further comprising an arbiter coupled to the plurality of entities to arbitrate at least one bus request from the plurality of entities.

6. ~~The system of claim 1, wherein the at least a portion of the memory of the at least~~ one entity is not reset when the at least one entity is the same entity that previously had control of the resource.

7. The system of claim 1, wherein the portion of the memory of the at least one entity is selectively reset when the at least one entity is different from an entity that ~~previously had control of the resource.~~

8. An integrated circuit for allowing at least one resource to be controlled by a processor among a plurality of processors, at least one processor among the plurality of processors including a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus; and

a switch mechanism, coupled to the central computing unit, to switch the control of the at least one resource, wherein a portion of the fast memory of at least one processor of the plurality of processors is selectively reset when the control of the at least one resource is switched.

9. The integrated circuit of claim 8, wherein the portion of the fast memory of the at least one processor is not reset when the at least one processor is the same processor that previously had control of the at least one resource.

10. The integrated circuit of claim 8, wherein the portion of the fast memory of the at least one processor is selectively reset when the at least one processor is different from a processor that previously had control of the at least one resource.

11. The integrated circuit of claim 8, wherein the switch mechanism is a hardware device.

12. The integrated circuit of claim 8, wherein the switch mechanism is a software switch.

13. The integrated circuit of claim 12, wherein the software switch is a Djikstra primitive.

14. The integrated circuit of claim 8, wherein the at least one resource is a hardware

resource.

15. The integrated circuit of claim 14, wherein the hardware resource is a memory.

16. The integrated circuit of claim 8, further comprising a communications channel controller coupled to the bus.

17. The integrated circuit of claim 8, wherein the at least one resource is a software resource.

18. The integrated circuit of claim 17, wherein the software resource is a data structure.

19. The integrated circuit of claim 8, wherein the fast memory is cache memory.

20. An integrated circuit for allowing at least one resource to be shared among a plurality of processors, at least one processor of the plurality of processors including a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus; and

a lock coupled to the central computing unit to reserve exclusive control of the at least one resource to a processor among the plurality of processors, wherein at least a portion of the fast memory of the processor of the plurality of processors is selectively reset when the processor of the plurality of processors has exclusive control of the at least one resource.

21. The integrated circuit of claim 20, wherein the portion of the fast memory of the processor is not reset when the processor is the same processor that previously had

exclusive control of the at least one resource.

22. The integrated circuit of claim 20, wherein the portion of the fast memory of the processor is selectively reset when the processor is different from another processor that previously had control of the at least one resource.

23. The integrated circuit of claim 20, wherein the lock is a hardware register.

24. The integrated circuit of claim 20, wherein the lock is a software semaphore.

25. The integrated circuit of claim 24, wherein the software semaphore is a binary semaphore.

26. The integrated circuit of claim 20, further comprising a communications channel controller coupled to the bus.

27. The integrated circuit of claim 20, wherein the fast memory is cache memory.

28. The integrated circuit of claim 27, wherein the cache memory is primary cache memory.

29. The integrated circuit of claim 27, wherein the cache memory is secondary cache memory.

30. A data structure in a machine-readable medium for allowing at least one resource to be shared among a plurality of processors, at least one processor of the plurality of processors including a fast memory, the data structure comprising:

a state for indicating that the at least one resource is under control; and

a first identifier for identifying a past processor that had exclusive control of the at least one resource.

31. The data structure of claim 30, wherein the data structure is a class, the data structure further comprising an act for resetting at least a portion of the fast memory of the present processor.

32. The data structure of claim 31, further comprising a second identifier for identifying the present processor that has exclusive control of the at least one resource.

33. The data structure of claim 32, further comprising an act for comparing the first identifier and the second identifier, and wherein the act for resetting the fast memory of the present processor being executed when the first identifier is different from the second identifier.

34. The data structure of claim 30, wherein the fast memory is cache memory.

35. The data structure of claim 30, further comprising a data type that is adapted to represent at least one portion of the at least one resource, wherein the data type includes at least one location of the at least one portion of the at least one resource and at least one dimension of the at least one portion of the at least one resource.

36. The data structure of claim 30, further comprising a list that includes at least one location of at least one portion of the at least one resource and at least one dimension of at least one portion of the at least one resource.

37. A method for allowing at least one resource to be shared among a plurality of processors, the method comprising:

obtaining exclusive control over the at least one resource by a present processor, the present processor including a fast memory;

identifying a past processor to obtain a first identity, wherein the past processor had exclusive control over the at least one resource; and

resetting selectively at least a portion of the fast memory of the present processor when the past processor is different from the present processor.

38. The method of claim 37, wherein identifying the present processor further comprises the fast memory as cache memory.

39. The method of claim 38, further comprising identifying a present processor to obtain a second identity, the present processor having exclusive control over the at least one resource, the present processor including a fast memory.

40. The method of claim 39, further comprising comparing the first identity and the second identity so as to determine if the present processor is different from the past processor.

41. The method of claim 37, wherein the progression of the method is in the order presented.

42. A method for scheduling access to at least one resource from among a plurality of processors, the method comprising:

obtaining access to the at least one resource from a requesting processor, the requesting processor including a cache memory;

excluding access to the at least one resource from the plurality of processors except for the requesting processor; and

resetting at least a portion of the cache memory of the requesting processor when

the requesting processor is different from a processor that previously had access to the at least one resource.

43. An integrated circuit for allowing at least one resource to be controlled by a processor among a plurality of processors, at least one processor among the plurality of processors including a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus;

a switch mechanism for switching the control of the at least one resource; and

a lock, in a cooperative relationship with the switching mechanism, for reserving exclusive control of the at least one resource to a processor among the plurality of processors, wherein at least a portion of the fast memory of the processor of the plurality of processors is selectively reset when the processor of the plurality of processors has exclusive control of the at least one resource.

44. The integrated circuit of claim 43, wherein the fast memory is cache memory.

45. The integrated circuit of claim 43, further comprising a communications channel controller coupled to the bus, wherein the communications channel controller is receptive to diverse communications protocols.

46. The integrated circuit of claim 43, wherein the cooperative relationship of the switch mechanism and the lock maintains cache coherency.

47. The integrated circuit of claim 43, wherein the at least a portion of the fast memory of the at least one processor is not reset when the processor is the same processor that previously had control of the at least one resource.

48. The integrated circuit of claim 43, wherein the portion of the fast memory of the processor is selectively reset when the processor is different from a processor that previously had control of the at least one resource.

49. An integrated circuit for allowing at least one resource to be controlled by a processor among a plurality of processors, at least one processor among the plurality of processors including a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus; and

a scheduler, coupled to the central computing unit, for scheduling the control of the at least one resource, wherein a portion of the fast memory of at least one processor of the plurality of processors is selectively reset when the at least one resource is under control.

50. The integrated circuit of claim 49, wherein the portion of the fast memory of the at least one processor is not reset when the at least one processor is the same processor that previously had control of the at least one resource.

51. The integrated circuit of claim 49, wherein the portion of the fast memory of the at least one processor is selectively reset when the at least one processor is different from a processor that previously had control of the at least one resource.

52. A system comprising:

a bus;

at least one resource coupled to the bus;

a plurality of processors coupled to the bus, at least one processor among the plurality of processors including a fast memory; and

a switch mechanism, coupled to the bus, to switch the control of the at least one

resource, wherein a portion of the fast memory of at least one processor of the plurality of processors is selectively reset when the control of the at least one resource is switched.

53. The system of claim 52, wherein the portion of the fast memory of the at least one processor is not reset when the at least one processor is the same processor that previously had control of the at least one resource.

54. The system of claim 52, wherein the portion of the fast memory of the at least one processor is selectively reset when the at least one processor is different from a processor that previously had control of the at least one resource.

55. The system of claim 52, wherein the switch mechanism is a hardware device.

56. The system of claim 52, wherein the switch mechanism is a software switch.

57. The system of claim 56, wherein the software switch is a Djikstra primitive.

58. The system of claim 52, wherein the at least one resource is a hardware resource.

59. The system of claim 58, wherein the hardware resource is a memory.

60. The system of claim 52, wherein the at least one processor includes a communications channel controller.

61. The system of claim 52, wherein the at least one resource is a software resource.

62. The system of claim 61, wherein the software resource is a data structure.

63. The system of claim 52, wherein the fast memory is cache memory.

64. A system comprising:

a bus;

at least one resource coupled to the bus;

a plurality of processors coupled to the bus, at least one processor of the plurality of processors including a fast memory; and

a lock to reserve exclusive control of the at least one resource to a processor among the plurality of processors, wherein at least a portion of the fast memory of the processor of the plurality of processors is selectively reset when the processor of the plurality of processors has exclusive control of the at least one resource.

65. The system of claim 64, wherein the portion of the fast memory of the processor is not reset when the processor is the same processor that previously had exclusive control of the at least one resource.

66. The system of claim 64, wherein the portion of the fast memory of the processor is selectively reset when the processor is different from another processor that previously had control of the at least one resource.

67. The system of claim 64, wherein the lock is a hardware register.

68. The system of claim 64, wherein the lock is a software semaphore.

69. The system of claim 68, wherein the software semaphore is a binary semaphore.

70. The system of claim 64, further comprising a communications channel controller coupled to the bus.

71. The system of claim 64, wherein the fast memory is cache memory.

72. The system of claim 71, wherein the cache memory is primary cache memory.

73. The system of claim 71, wherein the cache memory is secondary cache memory.

74. A system comprising:

a bus;

at least one resource coupled to the bus;

a plurality of processors coupled to the bus, at least one processor among the plurality of processors including a fast memory;

a switch mechanism to switch the control of the at least one resource; and

a lock, in a cooperative relationship with the switching mechanism, to reserve exclusive control of the at least one resource to a processor among the plurality of processors, wherein at least a portion of the fast memory of the processor of the plurality of processors is selectively reset when the processor of the plurality of processors has exclusive control of the at least one resource.

75. The system of claim 74, wherein the fast memory is cache memory.

76. The system of claim 74, wherein the at least one processor includes a communications channel controller, wherein the communications channel controller is receptive to diverse communications protocols.

77. The system of claim 74, wherein the cooperative relationship of the switch mechanism and the lock maintains cache coherency.

78. The system of claim 74, wherein the at least a portion of the fast memory of the at

least one processor is not reset when the processor is the same processor that previously had control of the at least one resource.

79. The system of claim 74, wherein the portion of the fast memory of the processor is selectively reset when the processor is different from a processor that previously had control of the at least one resource.